EE/CprE/Se 492 Weekly Report 4
2/28/25 - 3/13/25
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members
Calvin Smith – Accelerator Design lead
Camden Fergen – DevOps and Project Lead
John – Testing Lead
Nicholas – Harden and Verification lead
Levi – Communication Interfaces Lead

Weekly Summary

This week we worked on a lot of testing as well as getting more functionality into our CGRA. We were able to work on the CyDMA to load memory directly into the CyGRA and also, we were able to complete our dot product instruction and fully tested it. We will be testing the whole of the CyGRA soon and we also have been testing the rest of the components and the communication across the design.

Pask Week Accomplishments

- Calvin:
    - Completed components to interface CyGRA with the memory controller
    - Worked on FFT implementation for the CyGRA
- Camden:
    - Finished CICD pipeline for Verilog projects
    - Validated CICD pipeline on multiple test cases to ensure it works
    - Got up to speed on CyGRA to start full testing
- John:
    - Finished dot product instruction
    - Finished dot product testing
    - Adjusted code to facilitate future instructions
- Levi:
    - Working on FPGA testing to be ran on Xilinx boards in Durham 310 (WIP as of writing).
    - Progress hard to determine
- Nicholas:

- Completed memory system
- Debugged and fixed issues in current Caravel project
- Synthesized layout for PE Array
- Started looking into FPGA testing
- Wrote software to write firmware given a binary file containing RISC-V instructions

| Name | Individual Contribution | Hours this Week | Hours Cumulative |
|---|---|---|---|
| Calvin | • CyDMA<br>• Memory Splitter<br>• FFT | 10 | 120.044 |
| Camden | • Working CICD pipeline for Verilog repositories<br>• Understanding of CyGRA and how I want to approach testing | 10 | 110 |
| John | • Dot Product<br>• Testing<br>• CyGRA functionality | 20 | 130 |
| Levi | • FPGA Testing | 16 | 106 |
| Nicholas | • Bug Fixing Caravel<br>• OpenROAD synthesis of PE Array<br>• Completed memory system | 20 | 136 |

Plans for Upcoming Week

- Calvin:
  - Finish and test FFT instruction
- Camden:
  - Work on CyGRA testing with John to verify that the unit functions as expected
  - Port remaining CICD pipelines over to rest of repositories
  - Finish ARM CICD pipeline (test assembly instructions)

- John:
    - Help Calvin with FFT
    - Make sure we are testing properly and thoroughly
    - Help with the integration of CyDMA
- Levi:
    - GET FPGA TESTING WORKING!!! (get the pico processor fully implemented within the user_project_wrapper.v from chipforge)
    - Create/edit the makefiles needed for testing
    - Determine libraries needed for testing
    - Extract kernels from testbenches and derive a method for testing or get them compiling in full through the firmware dv/test method.
- Nicholas:
    - Test current Caravel design on an FPGA
    - Run benchmarks

Summary of weekly advisor meeting

Gave our weekly update about what we have done and what we are working on. Seemed happy with our progress; mentioned that we should make sure we are getting testing done soon. If needed, extract kernels from benchmarks to make sure that we are able to use the benchmarks to test our design.